GigaDevice Semiconductor Inc.

GD32C2x1 Software Development Guide

Application Note
AN235

Revision 1.0

（Jun. 2025）

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1. Overview

This document is specifically provided for the GD32C2x1xx series MCU, introducing how to set up and debug projects based on the GD32C2x1xx chip, as well as how to use each module. The purpose of this application note is to provide exemplary functional introductions to the peripheral resources on the GD32C2x1xx series MCU, enabling users to understand how to use the GD32C2x1xxx series chips for rapid software development.

Table 1-1. Applicable Products

Type	Model
MCU	GD32C231xx Series

2. Software feature development

2.1. Boot mode selection and configuration

When configuring the BOOT0 pin for startup from the main Flash, programming the original device becomes more convenient by checking the MFPE bit in the FMC_WS register. When the MFPE bit is set, the device is considered empty, and the bootloader starts from the System memory, allowing Flash programming at this point. During the loading of option bytes, if the content at address 0x0800 0000 is read as 0xFFFF FFFF, the MFPE flag will be set; otherwise, it will be cleared. After programming the original device, the MFPE flag can be cleared by either a power reset or setting the OBRLD bit in the FMC_CTL register, enabling the device to execute user code after a system reset. The MFPE flag can also be modified by software.

Note: If the device is programmed for the first time but option bytes are not reloaded, the device will still choose System memory as the boot area after a system reset.

The GD32C2x1 series provide three kinds of boot sources which can be selected by the BOOT0 pin and boot configuration bits BOOTLK, nBOOT1, SWBT0 and nBOOT0 in the User option byte. The details are shown in the following table. When SWBT0=0, the value on the BOOT0 pin is latched on the 4th rising edge of CK_SYS after a reset. It is up to the user to set the boot mode configuration after a power-on reset or a system reset to select the required boot source. When SWBT0=0, once the boot mode configuration have been sampled, they are free and can be used for other purposes.

Table 2-1. Boot modes

Selected boot area	Boot mode configuration				
	BOOTLK	nBOOT1 bit	BOOT0 pin	SWBT0 bit	nBOOT0 bit
Main Flash memory	0	x	0	0	x
System memory	0	1	1	0	x
Embedded SRAM	0	0	1	0	x
Main Flash memory	0	x	x	1	1
System memory	0	1	x	1	0
Embedded SRAM	0	0	x	1	0
Main Flash memory	1	x	x	x	x

2.2. Option byte modification

During the option byte modification process, ensure that the working environment is normal and stable, otherwise reset or power loss during the modification process will cause the chip to report OBERR and enter a strong protection state.

2.3. Flash emulate EEPROM

For more details about Flash emulate EEPROM refer to ***《AN213 GD32C2x1 系列 FLASH 模拟 EEPROM》***, ***《AN213 FLASH emulate EEPROM for GD32C2x1 series》***。

2.4. RCU usage instructions

Some peripherals have configurable clocks, allowing users to select specific clocks for configuration according to their needs. However, before configuring a peripheral clock, it should be ensured that the corresponding clock has been enabled and is running stably. For peripherals that support dynamic clock switching, it should also be ensured that the target clock is running stably before switching. The peripherals with configurable clocks are as follows:

1. ADC clock can be derived from CK_IRC48MDIV_PER or from CK_SYS clock divided by 2, 4, 6, 8, 10, 12, 14, 16, 32, 64, 128, or 256;
2. USART clock can be selected from CK_APB, CK_SYS, CK_IRC48MDIV_PER, or CK_LXTAL clock, and USART supports dynamic clock switching;
3. I2C clock can be selected from CK_APB, CK_SYS, or CK_IRC48MDIV_PER clock, and I2C supports dynamic clock switching;
4. I2S clock can be selected from CK_SYS, CK_IRC48MDIV_PER, or I2S_CKIN clock, and I2S supports dynamic clock switching;
5. RTC clock can be selected from LXTAL clock, IRC32K clock, or HXTAL clock divided by 32.

3. Revision history

Table 3-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Jun. 03, 2025

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